CLAIMS

[1] An integrated circuit for video/audio processing that processes video and audio signals, comprising:

a microcomputer block including a CPU;

a stream input/output block operable to receive/output video and audio streams to and from an external device, under the control of said microcomputer block;

a media processing block operable to execute media processing including at least one of compression and decompression of the video and audio streams inputted to said stream input/output block or outputted from said stream input/output block under the control of said microcomputer block;

an AV input/output block operable to convert the video and audio streams subjected to the media processing in said media processing block and output the video and audio streams to an external device, or acquire the video and audio signals from the external device and convert the video and audio signals into video and audio streams to be subjected to the media processing in said media processing block, under the control of said microcomputer block; and

a memory interface block operable to control data transfer between a memory and said microcomputer block, said stream input/output block, said media processing block and said AV input/output block, under the control of said microcomputer block.

[2] The integrated circuit for video/audio processing according to Claim 1,

wherein said microcomputer block, said stream input/output block, said media processing block and said AV input/output block are connected to said memory interface block by a dedicated data bus, and

the video and audio streams are exchanged through said

memory among said microcomputer block, said stream input/output block, said media processing block and said AV input/output block.

[3] The integrated circuit for video/audio processing according to Claim 2,

wherein said memory interface block is operable to relay the data transfer so that the data transfer between said memory and said microcomputer block, said stream input/output block, said media processing block and said AV input/output block is made in parallel.

[4] The integrated circuit for video/audio processing according to Claim 2,

wherein said microcomputer block, said stream input/output block, said media processing block and said AV input/output block have no buffer memory for buffering the video and audio streams.

[5] The integrated circuit for video/audio processing according to Claim 2,

wherein said microcomputer block, said stream input/output block, said media processing block and said AV input/output block store the video and audio streams in said memory and notify the other blocks of the storage.

[6] The integrated circuit for video/audio processing according to Claim 2,

wherein said stream input/output block has an interface unit operable to transmit and receive the video and audio streams to and from said external device, an encryption processing unit operable to encrypt or decrypt the video and audio streams transmitted and received, and a direct memory access control unit

operable to transfer data between said external device and said memory,

said media processing block has an instruction parallel processor which executes plural signal processing instructions in parallel, an accelerator which executes an arithmetic operation, and a direct memory access control unit operable to control the data transfer with said memory,

said AV input/output block has a graphics engine which executes graphics processing of image data, and a format conversion unit operable to convert the format of the video signal, and

said memory interface block has plural ports connected to said microcomputer block, said stream input/output block, said media processing block and said AV input/output block, and has a memory scheduler which adjusts the timing of data transfer at each of said plural ports.

[7] The integrated circuit for video/audio processing according to Claim 6,

wherein said microcomputer block further has at least one of a clock control unit operable to turn on/off the supply of a clock to said CPU and a power supply control unit operable to turn on/off the power supply.

[8] The integrated circuit for video/audio processing according to Claim 6,

wherein said media processing block further has a data parallel processor which executes an arithmetic operation on plural pieces of data in parallel.

[9] The integrated circuit for video/audio processing according to Claim 2, further comprising:

a signal line which connects said stream input/output block and said media processing block,

wherein said media processing block is operable to execute media processing of the video and audio streams inputted from said stream input/output block through said signal line or the video and audio streams to be outputted to said stream input/output block through said signal line.

[10] The integrated circuit for video/audio processing according to Claim 2,

wherein circuit elements and wiring between the circuit elements in said microcomputer block, said stream input/output block, said media processing block, said AV input/output block and said memory interface block are formed on a circuit layer and a first wiring layer, respectively, on a semiconductor substrate; and

said data bus is formed on a second wiring layer located above said first wiring layer.

[11] The integrated circuit for video/audio processing according to Claim 2,

wherein said integrated circuit for video/audio processing is used as a system LSI for plural different devices; and

the devices include a digital TV, a digital video recorder, a video camera and a portable telephone.

[12] The integrated circuit for video/audio processing according to Claim 11,

wherein assuming that one of said devices is designated as a first device and another as a second device and a process is shared by said integrated circuit for video/audio processing for the first device and said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by said microcomputer block of said integrated circuit for video/audio processing for the first device, the process is executed by said microcomputer block of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by said stream input/output block of said integrated circuit for video/audio processing for the first device, the process is executed by said stream input/output block of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by said media processing block of said integrated circuit for video/audio processing for the first device, the process is executed by said media processing block of said integrated circuit for video/audio processing for the second device; and

in the case where the process is executed by said AV input/output block of said integrated circuit for video/audio processing for the first device, the process is executed by said AV input/output block of said integrated circuit for video/audio processing for the second device.

[13] The integrated circuit for video/audio processing according to Claim 11,

wherein in the case where one of the devices is designated as a first device and another as a second device,

the CPU of said integrated circuit for video/audio processing for the first device and the CPU of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible with each other.

[14] The integrated circuit for video/audio processing according to Claim 11,

wherein said media processing block has an instruction parallel processor which executes plural signal processing instructions in parallel; and

in the case where one of the devices is designated as a first device and another as a second device,

the instruction parallel processor of said integrated circuit for video/audio processing for the first device and the instruction parallel processor of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible with each other.

[15] The integrated circuit for video/audio processing according to Claim 11,

wherein said media processing block has an instruction parallel processor which executes plural signal processing instructions in parallel; and

in the case where one of the devices is designated as a first device and another as a second device,

the core of the CPU of said integrated circuit for video/audio processing for the first device and the core of the CPU of said integrated circuit for video/audio processing for the second device have the same logic connection, and

the core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and the core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have the same logic connection.

[16] The integrated circuit for video/audio processing according to Claim 11,

wherein said media processing block has an instruction parallel processor which executes plural signal processing

instructions in parallel; and

in the case where one of the devices is designated as a first device and another as a second device,

the core of the CPU of said integrated circuit for video/audio processing for the first device and the core of the CPU of said integrated circuit for video/audio processing for the second device have the same mask layout, and

the core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and the core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have the same mask layout.

[17] The integrated circuit for video/audio processing according to Claim 11,

wherein in the case where one of the devices is designated as a first device and another as a second device,

the address of the control register for said stream input/output block, said media processing block, said AV input/output block and said memory interface block on the memory map of the CPU in said integrated circuit for video/audio processing for the first device is identical to the address of the control register for said stream input/output block, said media processing block, said AV input/output block and said memory interface block on the memory map of the CPU in said integrated circuit for video/audio processing for the second device.

[18] A method of designing and developing devices using the integrated circuit for video/audio processing according to Claim 1,

wherein the devices include a digital TV, a digital video recorder, a video camera and a portable telephone.

[19] The method of designing and developing devices according to Claim 18, wherein the design and development is performed in such a manner that:

assuming that one of the devices is designated as a first device and another of the devices as a second device and a process is shared by said integrated circuit for video/audio processing for the first device and said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by a microcomputer block of said integrated circuit for video/audio processing for the first device, the process is executed by a microcomputer block of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by a stream input/output block of said integrated circuit for video/audio processing for the first device, the process is executed by a stream input/output block of said integrated circuit for video/audio processing for the second device;

in the case where the process is executed by a media processing block of said integrated circuit for video/audio processing for the first device, said process is executed by a media processing block of said integrated circuit for video/audio processing for the second device; and

in the case where the process is executed by an AV input/output block of said integrated circuit for video/audio processing for the first device, the process is executed by an AV input/output block of said integrated circuit for video/audio processing for the second device.

[20] The integrated circuit for video/audio processing according to Claim 2,

wherein said AV input/output block is further operable to

generate a recording video signal by converting the resolution of the video signal converted from the video stream subjected to media processing by said media processing block or acquired from an external device, as well as generating field feature information indicating at least one of the in-field total and the inter-field difference of the video fields indicated by the recording video signal; and

said media processing block is further operable to access the field feature information and convert the recording video signal into a recording video stream.

[21] The integrated circuit for video/audio processing according to Claim 20, further comprising

a signal line which connects said media processing block and said AV input/output block,

wherein the field feature information is exchanged between said media processing block and said AV input/output block through said signal line.

[22] The integrated circuit for video/audio processing according to Claim 2,

wherein said media processing block executes, by time division, a multiplexing or demultiplexing process for the stream, a video data compressing or decompressing process, and an audio data compressing or decompressing process for one video/audio multiplex stream, as well as prohibiting the multiplexing or demultiplexing process for the stream from being executed plural times within a predetermined time.

[23] The integrated circuit for video/audio processing according to Claim 22,

wherein said media processing block has a virtual

multiprocessor functioning as plural logical processors by time division;

the multiplexing or demultiplexing process for said stream, the compressing or decompressing process for said video data, and the compressing or decompressing process for said audio data are executed by different logical processors, respectively, which are the function of said virtual multiprocessor; and

the logical processor for executing the multiplexing or demultiplexing process for said stream sleeps until the expiry of the time on a predetermined timer after completion of the processing of a predetermined unit of said stream.